DATE April 8, 1960

SUBJECT   Average Response Computer Program (ARC)

TO   PDP Distribution List   FROM   John C. Conley

This computer application program is written to pick out and display a weak signal which has been distorted by a high degree of noise. The signal, with noise, is fed into an analog to digital convertor for measurement and conversion to binary information. Successive measurements are made over the same portion of the input, added to the sum of previous samples, and stored in memory. The resultant sum is displayed after each sample and as the sample size increases the display shows the true signal with decreasing distortion.

This program is written for memory storage in registers 0-167 with sample storage in registers 170-1170. This is a sample and display of 512 points on each pass.

As explained in the operating instructions, the program has several variable features which control speed of operation and display characteristics. Continuous display, at any preassigned point, is possible for analysis and picture taking of waveform. Overall speed of the averaging process can be controlled by the sense switches. The display part of the program is time consuming and can be cut out for very rapid sampling and a display of the final results.

Operating Instructions

1) Read in binary format tape of ARC program.

2) Set or clear sense switches 1,2 and 3 as desired. See Note 1 for function of sense switches.

3) Set left nine and right nine bits of test word as needed. See Notes 1 and 2 for function of test word bits.

4) Set test address to zero.

5) Turn on signal source.

6) Push start switch on console.

Program will run and display 512 points on each pass. The program is controlled by a sync instruction from the input, such that each sample will be taken from the same starting point in the input source.

Note 1 - Function of sense switches

Sense switch 1 controls the speed with which a sample is made and so the number of cycles included in the 512 points.

SW 1 .. Set .. Fastest sample time

SW 1 .. Clear -- Delayed sampling - a delay is introduced between the measurement of each point. The length of this delay is specified by bits 9-17 of the test word.

Sense switch 2 controls the display of each sample taken.

SW 2 .. Set .. Points are displayed after each sample

SW 2 .. Clear .. Points are displayed after each X samples. X is determined by bits 9-17 of test word.

Sense switch 3 determines continuous or limited sampling.

SW 3 .. Set .. Samples are taken and displayed continuously until machine is stopped.

SW 3 .. Clear .. Stops sampling after X samples and displays continuously what is then in storage. X is in register 133, (Program is now set for 1000 samples.)

Note 2 - Function of test word bits

As explained in Note 1, test word bits 9-17 are used either to specify delay between points in a sample or the number of samples between displays depending on the setting sense switches 1 and 2.

Bits 0-8 specify the position of the first measured point, in a sample, after the sync signal is received by the computer. The more bits used the shorter the delay between sync signal and first measured point.

ARC

KEY	ADDRESS	INSTRUCTION	CODE	COMMENTS
A	0	JMP 133	60 0133	Start
	1	JSP src	62 0151	src sets initial address for storage
	2	CLA	76 0200)	Clear register con-
	3	DAC T	24 0145)	taining max scale factor
B	4	CLA	76 0200)	
	5	DAC&N	25 0150)	
	6	IDX N	44 0150)	Clear storage regis-
	7	SAS Y 52	52 0142)	ters before sampling
	10	JMP B	60 0004)	begins
cc	11	SZF 2	64 0020)	
	12	JMP H	60 0017)	Display after each sample
	13	LAT	76 2200)	Display after each X samples
	14	AND M	02 0155)	X in bits 9-17 of test word
	15	CMA	76 1000)	
	16	DAC dd	24 0041)	
H	17	JSP src	62 0151	
AB	20	IOT 20	73 0020	Analog sync instruc- tion
AC	21	LAT 76 22	76 2200)	
	22	AND S	02 0156)	(Delay in start of (sample in bits 0-8 (of test word
u	23	ADD 0	40 0141)	(
	24	SPA	64 0200)	(
	25	JMP U	60 0023)	(Delay some more
AD	26	IOT	73 0010)	
	27	RCL 9	66 3777)	Analog input-puts 6 bits in IO 0-5
	30	RCL 9	66 3777)	Put sign in AC-0
	31	SAR 6	67 5077)	Most significant
	32	SAR 6	67 5077)	bits in AC 13-17 with proper sign AC 0-12
	33 10	ADD&N	41 0150)	Add to previous
	34 10	DAC&N	25 0150)	responses and
	35 10	IDX N	44 0150)	store
	36 10	SAS Y	52 0142)	

KEY	ADDRESS	INSTRUCTION	CODE	COMMENTS
	37	JMP R	60 0043	Not finished
	40	JMP	60 0121	Last response
dd	41			Counter for X samples
bb	42			Counter for 1000 samples
R	43	SZF 1	64 0010)	
	44	JMP D	60 0026)	
	45	LAT	76 2200)	Sample at fastest
	46	AND M	02 0155)	rate delay between
	47	CMA	76 1000)	responses test word
	50	DAC F	24 0143)	bits 9-17 artificial
W	51	ISP F	46 0143)	expansion ends at
	52	JMP W	60 0051)	register 53
	53	JMP D	60 0026)	
E	54	JSP src	62 0151	Reset initial address for display
G	55	LIO&N	23 0150	Load response sum for display
	56	SIL	66 6000	
V	57	SIL P	66 6777	Scale factor
	60	LAC N	20 0150	Set up X axis in AC
	61	ADD X	40 0144	
	62	JMP	60 0163	Go to display point
AF	63	LAC&N	21 0150)	Check point for max scale factor
	64	SPA	64 0200)	
	65	CMA	76 1000)	
	66	SUB T	42 0145	Subtract present max
	67	SPA	64 0200	
	70	JMP L	60 0075	No new maximum
	71	LAC&N	21 0150	New maximum
	72	SPA	64 0200	
	73	CMA	76 1000	
	74	DAC T	24 0145	

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KEY	ADDRESS	INSTRUCTION	CODE	COMMENTS
L	75	IDX N	44 0150	
AG	76	SAS Y	52 0142	Check for lost point
	77	JMP G	60 0055	More points to display
	100	LAW-9	71 0011)	Last point, set
	101	DAC K	24 0157)	counter for maximum
	102	LAW 6000	70 6000)	scale number. Put
	103	DAP V	26 0057)	zero in scale register
Q	104	LAC T	20 0145)	
	105	RAL 1	66 1001)	
	106	DAC J	24 0146)	
	107	SPA	64 0200)	104-120 scales pres-
			)	ent maximum
aa	110	JMP cc	60 0011)	
	111	ISP K	46 0157)	
	112	JMP Z	60 0114)	
ab	113	JMP cc	60 0011)	max scaling is zero
Z	114	LAC Y	20 0057)	
	115	RAL 1	66 1001)	Put one shift in scale
	116	ADD A	40 0147)	
	117	DAP V	26 0057)	
	120	JMP	60 0166)	
	121	SZF 3	64 0030	Switch for continu- ous or limited sampling
	122	JMP ac	60 0160	Continuous sampling
	123	ISP bb	46 0042	Stop adding after 1000 samples
	124	JMP ac	60 0160	
	125	LAW 54	70 0054)	Set jump instruction
	126	DAP aa	26 0110)	for continuous display
	127	DAP ab	26 0113)	after 1000 samples
	130	ISP dd	46 0041	
	131	JMP H	60 0017	1000 not reached
	132	JMP E	60 0054	1000 reached - con- tinuous display
	133	LAW-1747	71 1747	Set counter for 1000 samples
	134	DAC bb	24 0042	bb is counter

KEY	ADDRESS	INSTRUCTION	CODE	COMMENTS
	135	LAW	70 0011)	Set jump location
	136	DAP aa	26 0110)	for continuous samp-
	137	DAP ab	26 0113)	ling
	140	JMP	60 0001	
O	141		00 1000	
Y	142		00 1170	End of storage
F	143			Counter for artifi- cial expansion
X	144		77 7207	Scale for X axis
T	145		00 0000	
J	146			
A	147		00 2000	
N	150		00 0170	Beginning storage register
src	151	DAF	26 0154)	Specify initial
	152	LAW	70 0170)	address for storage
	153	DAC N	24 0150)	of responses
	154	JMP	60	Exit
M	155		00 0777	Mask
S	156		77 7000	Mask
K	157			
ac	160	SZF Z	64 0020	Switch for sample display
	161	JMP E	60 0054	Display each sample
	162	JMP	60 0130	Display every X samples
	163	SAL 9	66 5777	
	164	DSP	73 0007	
	165	JMP AF	60 0063	
	166	LAC J	20 0146	
	167	JMP Q	60 0105	